AVR 300: Software TWI Master Interface

Features

- **Uses No Interrupts**
- **Supports Normal and Fast Mode**
- **Supports Both 7-bit and 10-bit Addressing**
- **Supports the Entire AVR Microcontroller Family**

Introduction

The need for a simple and cost effective inter-IC bus for use in consumer, telecommunications and industrial electronics, led to the developing of the TWI bus. Today the TWI bus is implemented in a large number of peripheral and microcontrollers, making it a good choice in low speed applications.

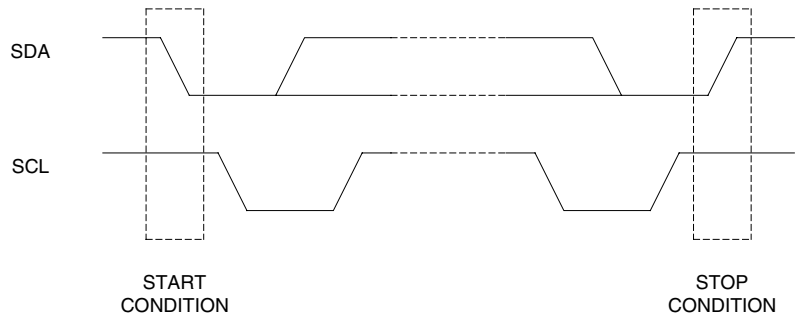
The AVR microcontroller family does not have dedicated hardware for TWI operation, but because of the flexible I/O and high processing speed, an efficient software TWI single master interface, can easily be implemented.

Theory of Operation

The TWI bus is a Two-wire synchronous serial interface consisting of one data (SDA) and one clock (SCL) line. By using open drain/collector outputs, the TWI bus supports any fabrication process (CMOS, bipolar and more).

The TWI bus is a multi-master bus where one or more devices, capable of taking control of the bus, can be connected. When there is only one master connected to the bus, this does not need to support handling of bus contentions and inter master access (a master accessing another master). Only master devices can drive both the SCL and SDA lines while a slave device is only allowed to issue data on the SDA line.

Figure 1. START and STOP Conditions



8-bit AVR® Microcontroller

Application Note

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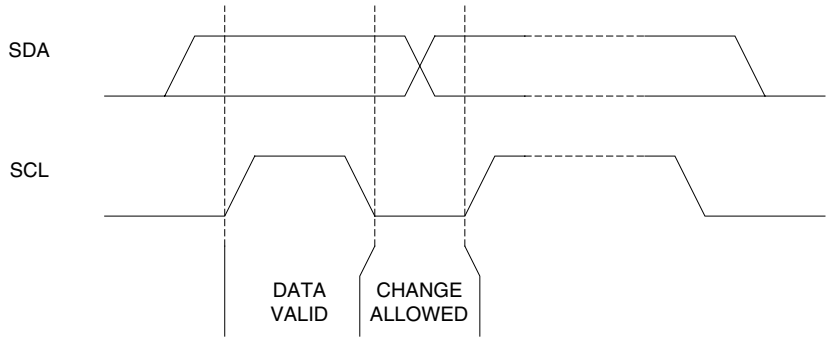
Data transfer is always initiated by a Bus Master device. A **high** to **low** transition on the SDA line while SCL is high is defined to be a START condition (or a repeated start condition). A START condition is always followed by the (unique) 7-bit slave address and then by a data direction bit. The Slave device addressed now acknowledges to the Master by holding SDA low for one clock cycle. If the Master does not receives any acknowledge, the transfer is terminated. Depending of the data direction bit, the Master or Slave now transmits 8-bit of data on the SDA line. The receiving device then acknowledges the data. Multiple bytes can be transferred in one direction before a repeated START or a STOP condition is issued by the Master. The transfer is terminated when the Master issues a STOP condition. A STOP condition is defined by a **low** to **high** transition on the SDA line while the SCL is high.

If a Slave device cannot handle incoming data until it has performed some other function, it can hold SCL low to force the master into a Wait State.

Figure 2. Bit Transfer on the TWI Bus



Change of data on the SDA line is only allowed during the low period of SCL as shown in Figure 2. This is a direct consequence of the definition of the START and STOP conditions. A more detailed description and timing specifications, can be found in [1].

Transferring Data

All transfer on the bus is byte sized. Each byte is followed by an acknowledge bit set by the Receiver. The slave address byte contains both a 7-bit address and a read/write bit.

Figure 3. Byte Transfer Formats

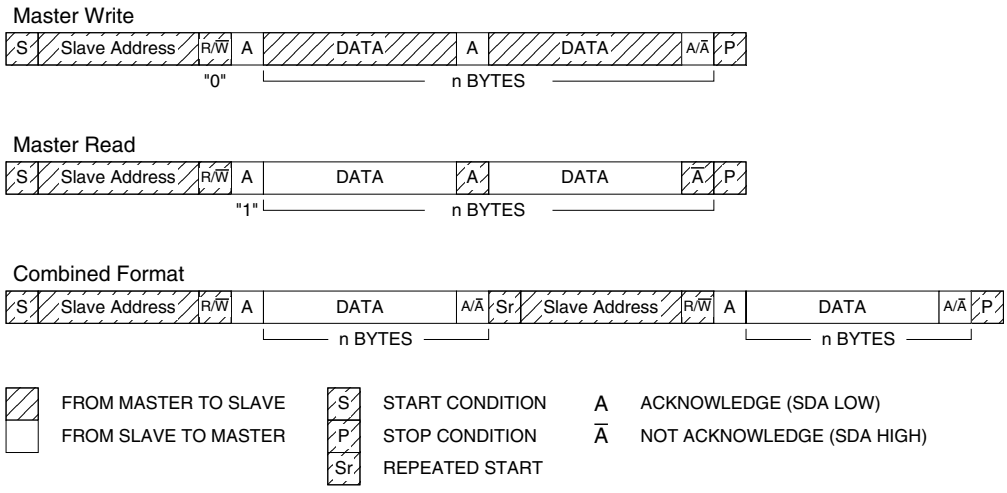


Figure 3 shows the valid data transfer formats. In the combined format, multiple data can be sent in any direction (to the same Slave device). A change in data direction is done by using a *repeated* START condition. Note that a Master read operation must be terminated by not acknowledging the last byte read.

Connection

Both TWI lines (SDA and SCL) are bi-directional therefore outputs must be of an open-drain or an open-collector type. Each line must be connected to the supply voltage via a pull-up resistor. A line is then logic high when none of the connected devices drives the line, and logic low if one or more is drives the line low.

Figure 4. Physical Connection to the TWI Bus

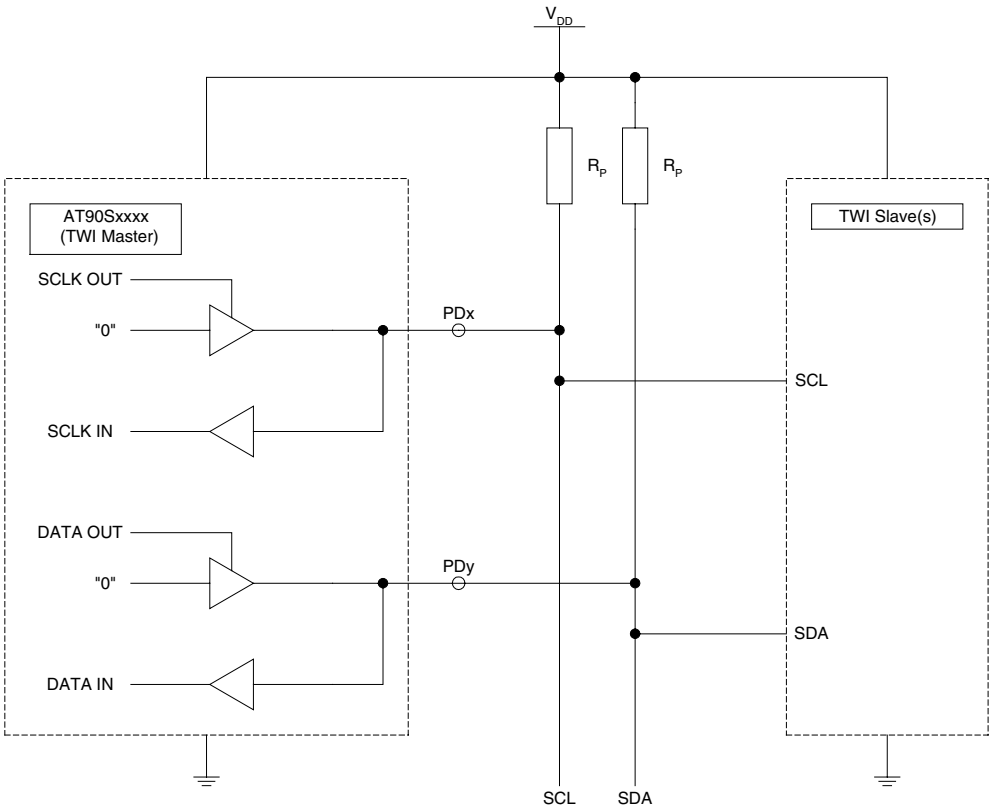


Figure 4 shows how to connect the AVR microcontroller to the TWI bus. The value of R_P depends on V_{DD} and the bus capacitance (typically 4.7 k).

Implementation

The only resources used by the TWI Master routines presented in this application, is the two pins for SCL and SDA on port D. Since the TWI bus is synchronous, the duty cycle and the period time to the Serial Clock Line (SCL) is not critical. Therefore it is not necessary to “fine-tune” the routines which would cause to an increase of program size.

There are two types of delays used in this implementation: quarter period and half period delays. For TWI in Normal mode (100 kHz), these delays must be $t_{quarter} > 2.5$ µs and $t_{half} > 5.0$ µs. For TWI in Fast mode (400 kHz) the parameters are $t_{quarter} > 0.6$ µs and $t_{half} > 1.3$ µs.

There is a large number of possible implementations of the delay loop. All the implementations depends on the MCU clock frequency. It is not possible to make a generalized version which is efficient for all clock speeds.

The following steps show how to choose the most efficient implementation of the delays:

1. Calculate the required number of clock cycles both delays:
   $n = t * f_{osc}$; $t = t_{quarter}$ and t_{half}, f_{osc} is MCU clock.
2. Use n to chose one of the following methods for both delays.

n	Delay method
< 1	Remove all calls to the delay routine
1 < n < 2	Replace all calls to the delay routine with one “nop” instruction
2 < n < 3	Replace all calls to the delay routine with an “rjmp 1” instruction
2 < n < 7	The delay routine should consist of one “ret” instruction only

> 7	Use the following routine :
	`ldi TWIdelay, 1+ (n-7)/3`
	`loop: dec TWIdelay`
	`brne loop`
	`ret`
	`(this routine is used in the program code!)`

TWI Subroutines

“TWI_init”

Initializes SCL and SDA lines. The SCLP and SDAP constants located top of the program code, chooses the pin number on port D. It is possible to use any pins on any port by changing the program code if required.

All the port D initialization can be put in this subroutine to reduce code size.

“TWI_start”

Generate start condition and sends slave address. All data transfer must start with this subroutine. When a transfer is done the “TWI_end” must be called. *When the bus is free (after “TWI”_end is called) all registers are free for other usage.*

Parameter	Value
Code Size	3
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :3 • Global Registers :1

Register	Input	Internal	Output
r16		“TWIdelay” – Delay Loop Counter	
r17		“TWIdata” – Transmit buffer	
r18	“TWIadr” – Slave address and transfer direction (global)		

"TWI_rep_start"

Generate repeated start condition and sends slave address. A repeated START can only be given after a byte has been read or written.

Parameter	Value
Code Size	5
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :3 • Global Registers :1

Register	Input	Internal	Output
r16		"TWIdelay" – Delay Loop Counter	
r17		"TWIdata" – Transmit buffer	
r18	"TWIadr" – Slave address and transfer direction (global)		

"TWI_write"

Writes data (one byte) to the TWI bus. This function is also used for sending the address.

Parameter	Value
Code Size	16
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :2 • Global Registers :None

Register	Input	Internal	Output
r16		"TWIdelay" – Delay Loop Counter	
r17	"TWIdata" – Data to be written		

"TWI_get_ack"

Get slave acknowledge response. The reason for separate this subroutine from the "TWI_write" routine is to get a more readable program code.

Parameter	Value
Code Size	11
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :1 • Global Registers :None

Register	Input	Internal	Output
r16		"TWIdelay" – Delay Loop Counter	

Figure 5. “TWI_start”, “TWI_rep_start”, “TWI_write”, and “TWI_get_ack” Flow Chart

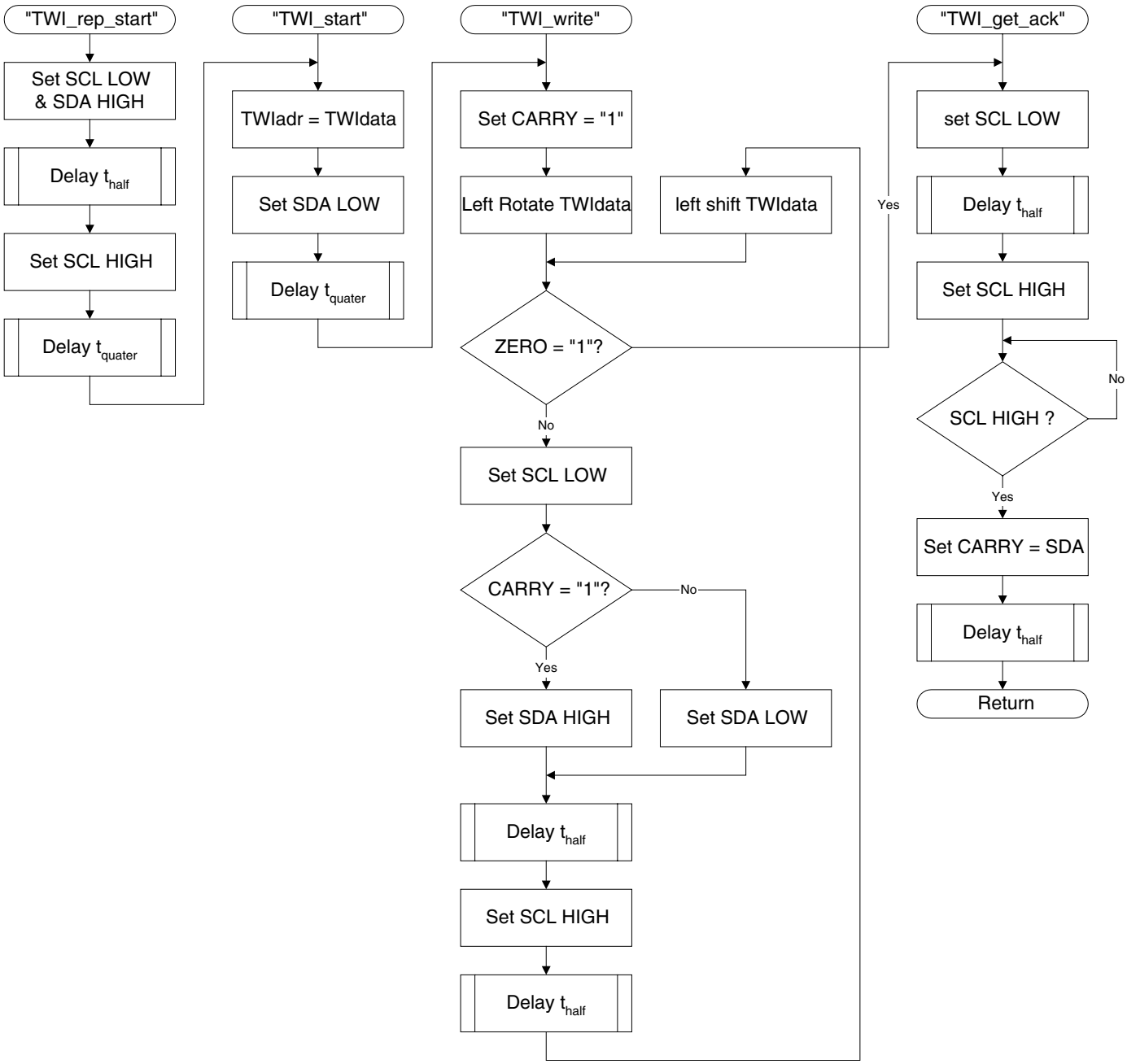


Figure 5 shows the flow chart for “TWI_start”, “TWI_rep_start”, “TWI_write”, and “TWI_get_ack”. These subroutines shares program code to reduce size.

"TWI_read"

Reads data (one byte) from the TWI bus.

Parameter	Value
Code Size	11
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :3 • Global Registers :1

Register	Input	Internal	Output
r16		"TWIdelay" – Delay Loop Counter	
r17			"TWIdata" – Received data
r19		"TWIstat" – Store acknowledge bit (global)	

"TWI_put_ack"

Put an acknowledge bit depending on carry flag is set or not. Separating this subroutine from the "TWI_read" routine is convenient for the user if a acknowledge is based on the result of the read operation.

Parameter	Value
Code Size	12
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :2 • Global Registers :1

Register	Input	Internal	Output
r16		"TWIdelay" – Delay Loop Counter	
r19		"TWIstat" – Acknowledge bit (global)	

Figure 6. “TWI_read” and “TWI_put_ack” Flow Chart

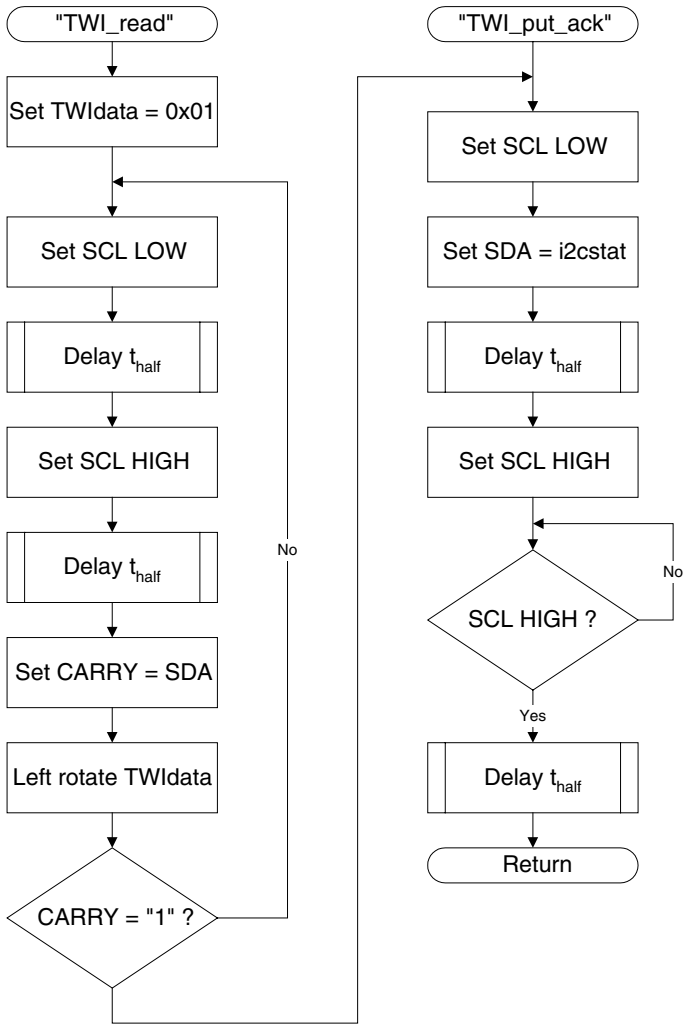


Figure 6 shows the flow chart for “TWI_read” and “TWI_put_ack”. These subroutines shares program code to reduce size.

“TWI_stop”

Generate stop condition. When a transfer is done the “TWI_end” must be called. When the bus is free (after “TWI”_end is called) all registers are free for use.

Parameter	Value
Code Size	8
Execution Cycles	N/A
Register Usage	• Low Registers :None • High Registers :1 • Global Registers :None

Register	Input	Internal	Output
r16		“TWIdelay” – Delay Loop Counter	

Figure 7. “TWI_stop” Flow Chart

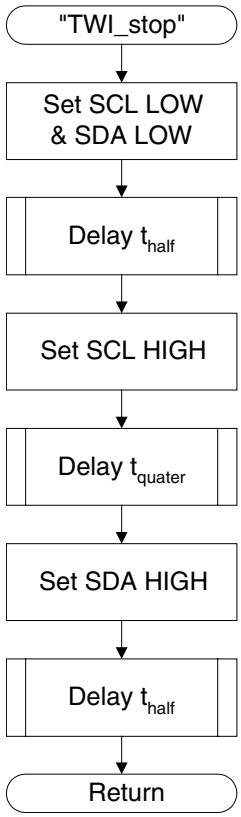


Figure 7 shows the flow chart for “TWI_stop”.

“TWI_do_transfer”

The “TWI_do_transfer” routine is implemented for convenience only. It uses the direction bit from the last address byte send, to decide whether to call the “TWI_read” or the “TWI_write” routine.

Tips and Warnings

The main loop in the program shows an example of reading and writing data to a 256-byte SRAM. This is a simple demonstration of how to use the TWI routines. Typically the reading and writing of SRAM will be implemented as functions calls, but since there is a large variety of slave implementations and ways of accessing them, the making this type of function calls is left for the user.

Warning! Do not change the order of the TWI routines. Most routines expects to be followed by a another specific TWI routine to work correctly.

Conclusion

This application note shows how to implement a master TWI interface on any AVR microcontroller device. This by using a minimum of resources. Since no interrupts are used in the implementation, these are free for other applications. It is also possible to use the TWI interface inside interrupts.

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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